COMPLEMENTARY A-Si:H/ORGANIC TFT CIRCUITS

By

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DEPARTMENT OF ELECTRICAL ENGINEERING

Indian Institute of Technology Kanpur

MAY, 2002

Complementary A-Si:H / Organic TFT Circuits

A Thesis Submitted
in Partial Fulfillment of the Requirements
for the Degree of

Master of Technology

By

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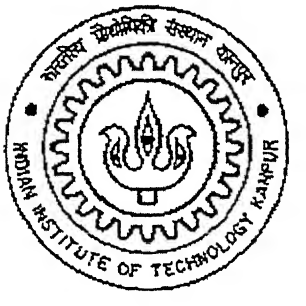

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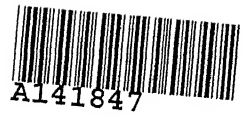

CERTIFICATE

This is to certify that the work presented in the thesis titled **"Complementary A-Si:H / Organic TFT Circuits"**, by Dharmesh kumar Sonkar (Roll No Y010411) has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

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ABSTRACT

This thesis present an estimate of performance that can be obtained from complementary CMOS circuits built using N-type amorphous Silicon TFT and P-type organic TFT (pentacene) The results from this work show that although basic gates with good static characteristic can be designed, the dynamic response is inferior by atleast three order of magnitude due to the poor mobility of carriers in both amorphous Silicon and Organic TFTs Results from more complicated circuits such as a simple 8-bit microprocessor indicate that the clock speed is lower than a bulk silicon circuit of comparable geometry by again three orders of magnitude

ACKNOWLEDGMENT

It gives me immense pleasure to express my heartful gratitude and sincere thanks to Dr B Mazhari for his inspiring guidance and encouragement at every stage of this work He has been very understanding and affectionate towards me He provided me with numerous valuable, innovative and constructive suggestions, without which this work would not have been possible I would also like to thanks Dr R Sharan and other instructors who have taught me various courses during the academic program

I am extremely grateful to my parents, elder brother, relatives and friends for their love, support, blessings and encouragement I am also thankful to Bhasker, Abhishek for their help in my thesis

My stay at IIT Kanpur has been very productive for me and I carry with me a happy memory of this place

May 2002 Dharmesh Kumar Sonkar

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Thin Film Transistor:

Thin-film transistors have recently attracted a considerable attention in many areas of modern electronics With process parameter optimization, small-grain TFT's yield good gate voltage swings and ON/OFF current ratios, allowing them to be used in a wide variety of potential applications, such as high-density SRAM's and DRAM's, three-dimensional integrated circuits, and switching elements in large-area flat panel displays Displays used in electronics such as watches, cell phones, PDAs, and pagers do not require high performance, and moving to a cheaper process can save considerable-manufacturing cost Many organizations are attempting to develop fully integrated displays (with integrated addressing circuitry) to eliminate the high-cost, low-yield driver attachment process currently used

1.1.1 Organic Thin Film Transistor:

Thin film transistors using organic semiconductors as the active layer material have received considerable attention in recent years The use of organic semiconductor as the active layer in TFTs may offer processing advantage over conventional thin film active layer materials like hydrogenated amorphous silicon (a-Si H) including reduced processing temperature This allows the use of inexpensive substrates of arbitrary size

including glass or polymers. Potential applications for organic TFTs include pixel access devices in active matrix liquid crystal displays, integrated pixel devices in all organic emissive displays, and low cost electronics for smart cards. It can also be used as switching devices for logic gates and memory arrays and large-area sensor arrays.

1.1.2 Amorphous-Si Thin Film Transistor:

One of the significant features of the a-Si TFT is its large on/off ratio defined as the ratio of on-state to off-state channel conductance. Because of this favorable characteristic, a-Si TFT's have been thought to be suitable as the switching elements of a matrix circuit of a liquid crystal display (LCD). As the switching element in active matrix LCD, the semiconductors such as single-crystal Si, polycrystalline Si, CdSe, and Te have been studied. Among these devices, a-Si is one of the most promising semiconductors satisfying the requirements for thin-film transistors for LCD.

1.2 literature review:

It appears increasingly likely that organic thin film transistors will find application, not only as pixel access elements in low cast active matrix displays, but also to integrate logic circuitry and memory arrays into low cast electronic products such as smart cards, smart price and inventory tags, and large-area sensor arrays [1].

Organic TFT's of pentacene have previously shown electrical characteristics comparable to those obtained with hydrogenated amorphous silicon devices, including field effect mobility as large as 1.5 cm^2/V-s and on/off current ratio larger than 10^8 [2].

Organic TFT's, fabricated on borosilicate glass showed excellent electrical characteristics, including field-effect mobility as large as 1.7 cm^2 /V-s, on/off current ratio larger than 10^8, and sub threshold slope as low as 0.4 V/dec [3].

Highest field-effect mobility (μ) values measured from OTFTs as reported in the literature annually from 1986 through 2000 is listed in Table 1 on the next page[4, 5].

Table 1

Year	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Material (deposition method) (v) = vacuum deposition (s) = from solution	I_{on}/I_{off}*	W/L
1983	Minimal, not reported (NR)	Polyacetylene (s) (demonstration of field effect in an OTFT)	NR	200
1986	10^{-5}	Polythiophene (s)	10^3	NR
1988	10^{-4}	Polyacetylene (s)	10^5	750
	10^{-3}	Phthalocyanine (v)	NR	3
	10^{-4}	Poly(3-hexylthiophene) (s)	NR	NR
1989	10^{-3}	Poly(3-alkylthiophene) (s)	NR	NR
	10^{-3}	α–ω-hexathiophene (v)	NR	NR
1992	0.027	α–ω-hexathiophene (v)	NR	100
	2×10^{-3}	Pentacene (v)	NR	NR
1993	0.05	α–ω-di-hexyl-hexathiophene (v)	NR	100–200
	0.22†	Polythienylenevinylene (s)	NR	1000
1994	0.06	α–ω-dihexyl-hexathiophene (v)	NR	50
1995	0.03	α–ω-hexathiophene (v)	$>10^6$	21
	0.038	Pentacene (v)	140	1000
	0.3	C_{60} (v)	NR	25
1996	0.02	Phthalocyanine (v)	2×10^5	NR
	0.045	Poly(3-hexylthiophene) (s)	340	20.8
	0.13	α–ω-dihexyl-hexathiophene (v)	$>10^4$	7.3
	0.62	Pentacene (v)	10^8	11
1997	1.5	Pentacene (v)	10^8	2.5
	0.05	Bis(dithienothiophene) (v)	10^8	500
1998	0.1	Poly(3-hexylthiophene) (s)	$>10^6$	20
	0.23	α–ω-dihexyl-quaterthiophene (v)	NR	1.5
	0.15	Dihexyl-anthradithiophene	NR	1.5
2000	0.1	n-decapentafluoroheptyl-methylnaphthalene-1,4,5,8-tetracarboxylic diimide (v)	10^5	1.5
	0.1	α–ω-dihexyl-quinquethiophene (s)	NR	NR

*Values for I_{on}/I_{off} correspond to different gate voltage ranges and thus are not readily comparable to one another. The reader is encouraged to read the details of the experiments in the cited references.

†This result has not yet been reproduced.

The complementary inverters were made by interconnecting the n-channel a-si and p-channel α-6T [5]. These complementary circuits show large voltage gain, excellent logic level conservation, and low static power dissipation. These inverters can operate at supply voltage as low as 7 V. The n-channel a-si TFTs were fabricated on glass substrates. The channel dimensions of the TFTs are W=8 μm, L=9μm. The p-channel α-6T TFTs were made on n-type Si wafers, the channel dimensions of the p-channel transistors are W=250μm, L=25μm. The a-Si TFTs has a field effect mobility of 0.1-1 cm^2/V-s, and α-6T TFTs has a field effect mobility of 0.01-0.03 cm^2/V-s. The threshold voltages are ~ 4 V and 0.2 V respectively.

1.3 Motivation of the thesis:

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFT's) and organic thin-film transistors (OTFT's) have attracted an increasing attention over the past few years due to their promising potential for applications involving large-area integration such as solar cell, image Sensor and matrix addressing of liquid-crystal display. Although hydrogenated amorphous silicon has ambipolar transport characteristics and can be operated in both p-channel and n-channel mode, p-channel a-Si:H TFTs have inferior characteristics compared with n-channel devices, and complementary integrated circuits using only a-Si:H transistors have not demonstrated useful performance. Most organic thin film semi-conductors, on the other hand, operate only in p-channel mode, although a small number of n-type organic semiconductors have been identified and all-organic complementary integrated circuits have recently been demonstrated. A low-cost manufacturing process for complementary inorganic/organic integrated circuits using hydrogenated amorphous silicon n-channel TFTs and pentacene p-channel TFTs have been developed.

1.4 Organization and plan of the thesis:

The thesis is organized in four chapters. In **chapter 2,** brief overviews of organic thin film transistors and A-Si thin film transistors have been given. This chapter describes the modeling of a-Si TFT and Pentacene TFT. **Chapter 3** describes the design and simulations of basic gate circuits like Inverter, NAND, NOR etc. with their delay characteristics. **Chapter-4** deals the results obtained from the synthesis of larger circuits such as multiplier, adder, microprocessor etc. **Chapter 5** summarizes the thesis and gives some suggestion for the future work.

To design and simulate logical circuits using Pentacene p-channel TFT and a-Si n-channel TFT, we needs a proper model for these two TFTs. We will design some basic gate circuits using these models. Simulating these logical gate circuits for different capacitive loads, we will generate a technology library used for synthesis. And finally we will synthesize some larger circuit.

CHAPTER 2

A-SI and PENTACENE TFT Models

2.1 Organic Thin Film Transistor:

Organic TFTs provide two principle advantages over thin film transistors based on inorganic semiconductors - they can be fabricated at lower temperature and, potentially, at significantly lower cost. Low process temperatures in particular may allow organic TFTs to be integrated on inexpensive plastic substrates, rather than glass. The prospect of flexible, unbreakable, extremely low-weight flat panel displays at relatively low cost has spurred a number of manufacturers and government agencies to consider plastic displays, imagers, and detectors for a variety of military, medical, industrial, and consumer applications.

Organic TFTs may also allow simple integrated circuits to be fabricated at extremely low cost, for applications such as radio-frequency price labels, identification tags, and smart cards. The carrier field-effect mobility larger than 1 cm^2 /V-s have been obtained in pentacene organic TFT's. In addition to large carrier mobility, a large on/off current ratio is required for TFT's to be useful as pixel-addressing devices in active-matrix displays. Small TFT sub threshold slope and near-zero threshold voltage are also important to reduce the power consumption of an integrated circuit or display. Finally, to address organic light emitters in all-organic emissive displays, TFT's must be able to drive fairly large drain currents.

All transistors and circuits were fabricated using polyethylene terephthalate (PET) film as the polymeric substrate material and borosilicate glass as the glass substrate material using the device structure shown in below

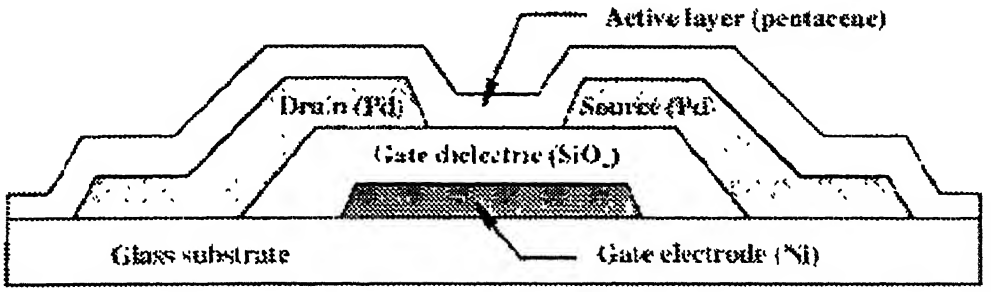

Fig 2 1.1 Pentacene thin film transistor on glass substrate

Low power consumption is an essential prerequisite for many potential organic TFT applications, and devices with low sub-threshold slope and near-zero threshold voltage are desirable

Since many organic semiconductors have p-type conductivity, they can also be used in a complementary integrated circuit technology combining n-channel hydrogenated amorphous silicon TFTs with p-channel organic TFTs Complementary thin film integrated circuit technology, analogous to silicon CMOS, is of particular interest for portable applications, where low power consumption is important.

2.2 Amorphous Silicon Thin Film Transistor:

Attractive advantages of amorphous silicon include its low temperature deposition and fabrication processes, which are compatible with low-cost glass substrates and standard metal-nitride semiconductor (MNS) integrated circuits, and capability of being deposited on a large area. Properties of a-Si H are quite different from those of crystalline material A-Si H is a direct-gap semiconductor with the energy gap close to 1 7 eV and electron and hole band mobilities are of the order 10 cm^2/V-s. It has a much larger absorption coefficient of light than crystalline silicon. The most important

are quite different from those of crystalline material. A-Si:H is a direct-gap semiconductor with the energy gap close to 1.7 eV and electron and hole band mobilities are of the order 10 cm^2/V-s. It has a much larger absorption coefficient of light than crystalline silicon. The most important difference between a-Si:H and a crystalline semiconductor is the presence of a large number of localized states in the energy gap.

Depending on the deposition sequence, a-Si:H TFTs can be classified into: (1) staggered, in which the gate dielectric layer is deposited on top of the a-Si:H layer, and (2) inverted structure, in which the gate dielectric is deposited first. The latter includes

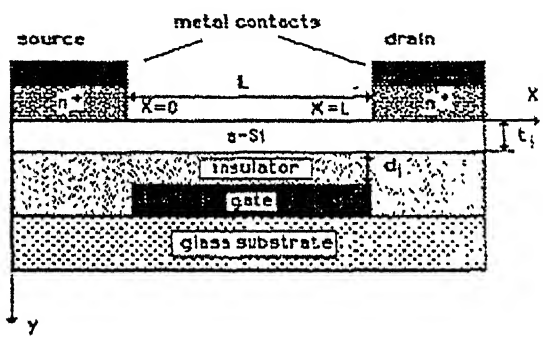

Fig 2.2 Schematic diagram of a-Si thin film transistors

the bilayer and the trilayer TFTs. In staggered structure the source/drain and gate contacts are on the opposite side of the semiconductor, whereas in coplanar source, drain and gate are on the same side of the semiconductor. Usually, a-Si:H TFT's are fabricated "inverted"; i.e., with the gate at the bottom because it is easier to obtain a good device when the dielectric is deposited first, While coplanar is a typical structure for polycrystalline silicon (poly-Si) TFT and metal oxide silicon field effect transistor (MOSFET).

2.3 Model for a-Si:H N-channel and pentacene P-channel TFTs:

For a-Si thin film transistors, a model as implemented in aim-spice circuit simulator [7] has been used The model parameter values are given in the **Appendix [A]**

2.3.1 A-Si:H N-channel TFT Model: The n-channel a-Si TFTs were fabricated on glass substrates A typical I_{DS} vs V_{DS} characteristic of a-Si NMOS is shown in fig 2.3 1 The threshold voltage of the TFT is 2 7V and oxide thickness is 170nm [6] The a-Si TFT has a field effect mobility of 1 cm^2/V s, which is the typical range for this material

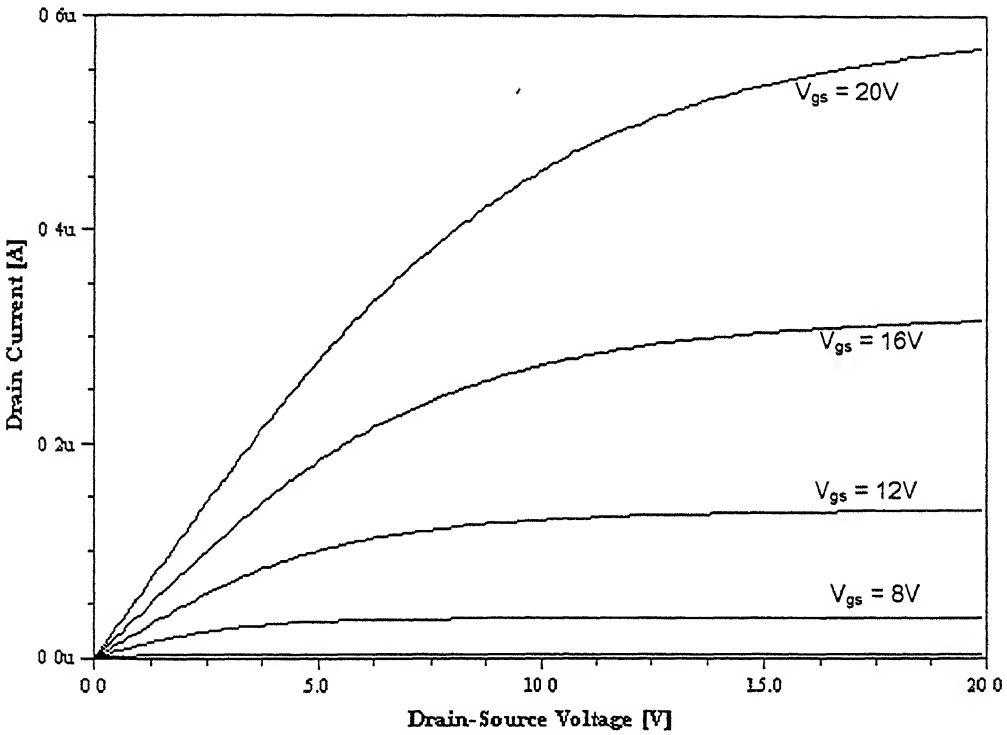

Fig 2 3 1 Current – voltage characteristics of an a-Si TFT with W/L = 1μm/1μm

And I_D Vs V_{GS} is shown in fig 2.3 2 below The threshold voltage is shown in figure

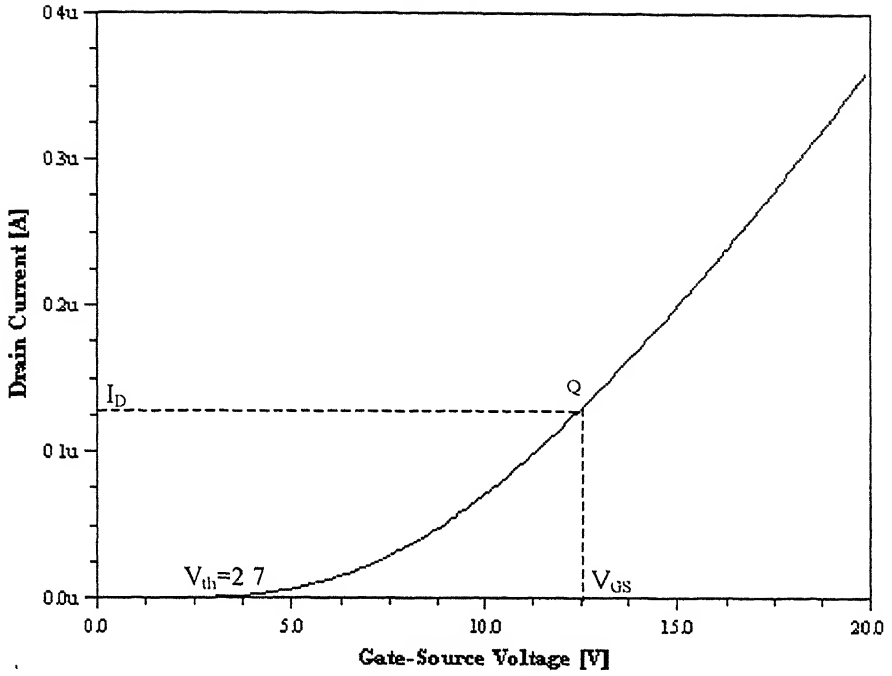

Fig 2 3 2 I_D-V_{GS} characteristics of a-Si TFT

2.3.2 Pentacene PMOS Model: The model for pentacene TFT was taken same as that of amorphous Silicon However, its parameters are determined by fitting the experimental data with the model These parameters are given in the **Appendix [A]** The curve with this model is shown in fig 2.3.3.

This figure shows a typical I_{DS} vs V_{DS} characteristic of Pentacene TFT The threshold voltage is –2V and oxide thickness is 170nm **[3]** Drain Current Vs Gate-Source is also shown in fig 2 3.4 The field effect mobility of Pentacene is 1.1 cm^2/Vs The device has $W/L = 240\mu m/44\mu m$

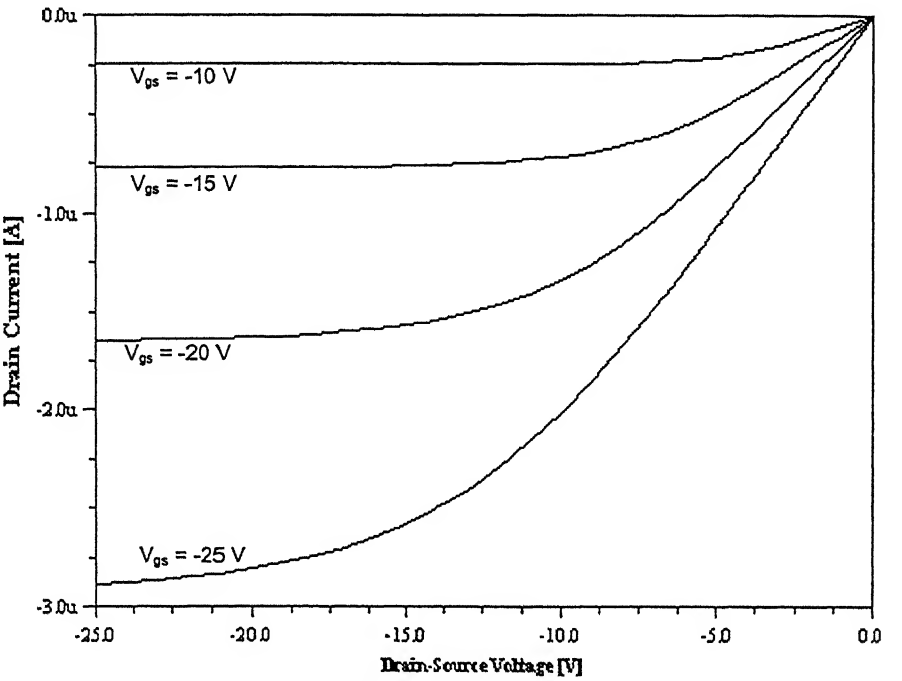

Fig 2.3.3 Current – voltage characteristics of an Pentacene TFT

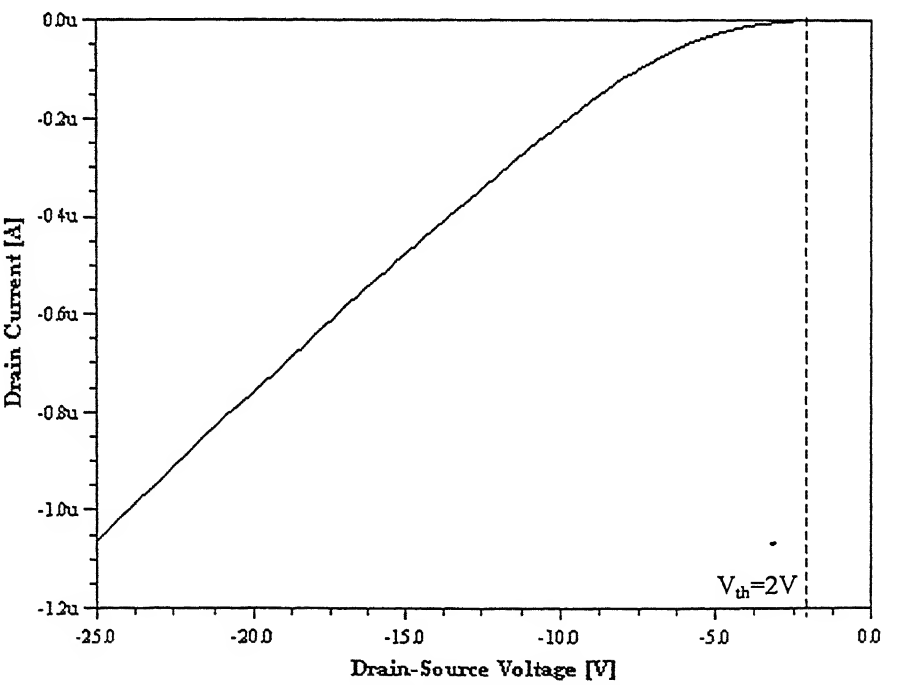

Fig 2.3.4 I_D-V_{GS} characteristics of Pentacene TFT

The characteristics of the Pentacene PMOS used for the design of digital circuits is

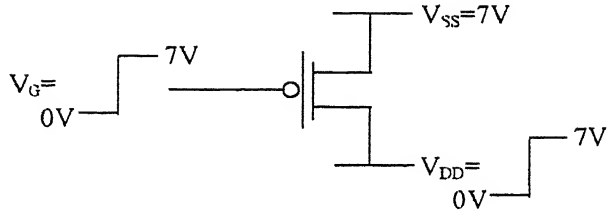

Fig 2 3.5 Pentacene PMOS

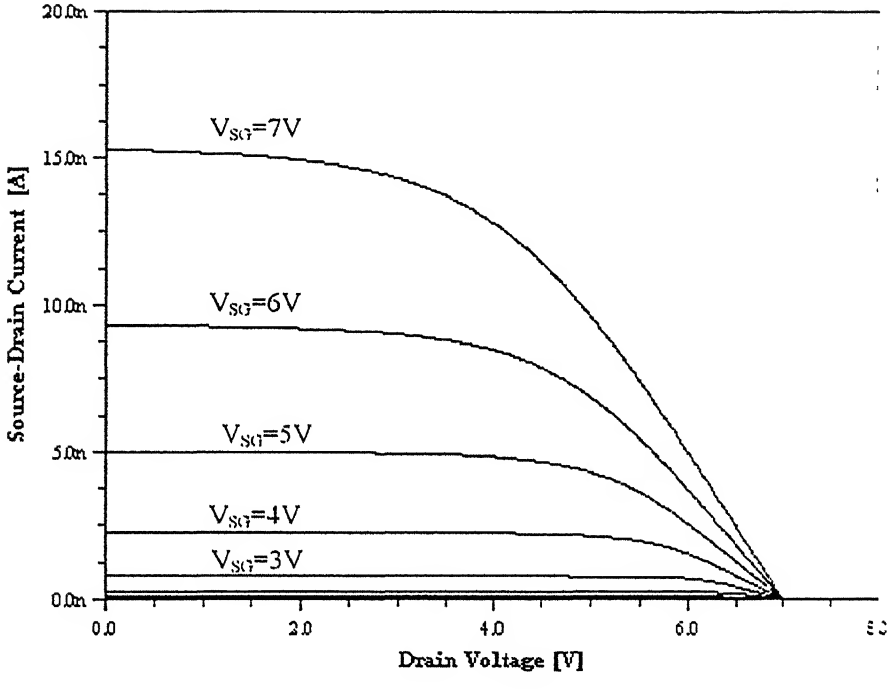

Fig 2.3 6 Current – voltage characteristics of an Pentacene TFT with W/L = 1μm/1μm

Design of digital circuits is described in next chapter.

CHAPTER 3

Design of Basic Gates

3.1 Inverter circuit:

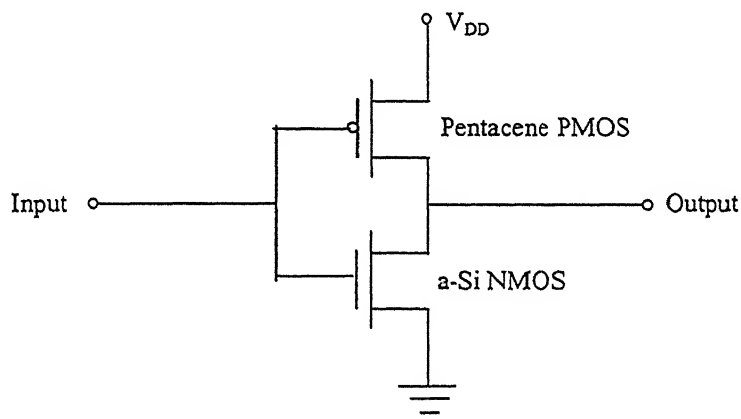

Fig 3.1.1 Inverter circuit configuration. The p-channel is of Pentacene and n-channel is of a-Si.

A complementary CMOS inverter realized by the series connection of a p-channel Pentacene TFT and n-channel a-Si TFT, described in previous chapter, is shown in above figure 3.1.1. The channel dimensions of the a-Si n-channel TFT are W=1μm, L=1μm and of the Pentacene p-channel TFT W=1μm, L=1μm. The field effect mobility of amorphous silicon TFT and Pentacene TFT have taken as 1 cm^2/V-s. The threshold voltage of a-Si and Pentacene TFTs are 3.8 and –2 respectively. The channel dimensions and the threshold voltages of the n-channel and p-channel transistors were chosen so that the transfer characteristics became symmetrical.

When the input is at V_{DD}, the n-channel TFT will be on and p-channel TFT will be off but a small leakage current will still flow through p-channel TFT. Similarly when input is at ground a small leakage current continues to flow through n-channel TFT. The result of these small leakage current is that V_{OH} is slightly less than V_{DD} and V_{OL} is slightly larger than 0.

Noise Margin: Noise Margin is a parameter closely related to the input-output characteristics. This parameter allows determining the allowable noise voltage on the input of a gate so that the output will not be affected. The specification most commonly used to specify noise margin (or noise immunity) is in terms of two parameters: NM_H (HIGH noise margin) and NM_L (LOW noise margin). The voltages V_{IL}, V_{IH}, V_{OH}, V_{OL} and V_M are described in the figure 3.1.2.

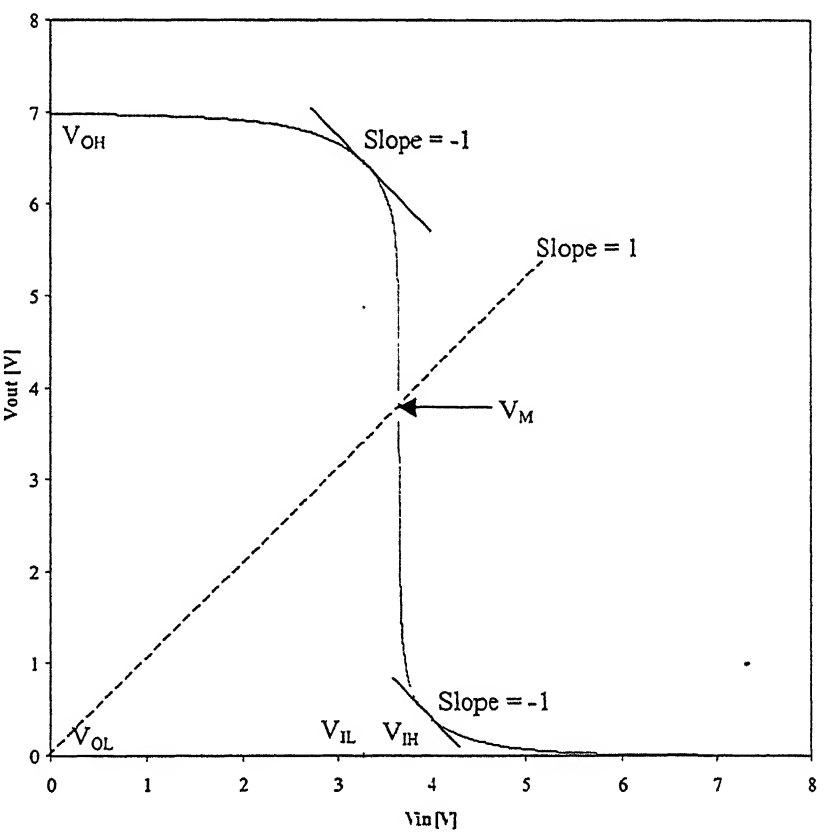

Fig 3.1.2 Transfer characteristics of a typical inverter

The inverter was tested under a variety of bias conditions. The supply voltage was varied in the range 5-10V and the transfer characteristics measured in each case. The corresponding values of V_{OH}, V_{OL} and V_M (or V_{inv}) are listed in the table 3.1 below. The transfer characteristics for the supply voltage of 7V was found the most suitable, and the curve is shown in figure 3.1.3. These all results are for the a-Si n-channel TFT threshold voltage of 3.8V and pentacene p-channel TFT threshold voltage of –2V.

Table 3.1

V_{DD} (V)	V_{OH} (V)	V_{OL} (V)	V_M (V)
5	4.97	0.026	2.94
6	5.98	0.015	3.52
7	6.986	0.008	4.05
7.5	7.487	0.009	4.3
8	7.99	0.006	4.54
9	8.99	0.002	4.99
10	9.995	0	5.44

As it can be seen that increasing the threshold voltage of n-channel TFT, shifts the curves towards right. The results of the simulation are shown in figure 3.1.3 for different values of the threshold voltage of n-channel TFT.

For V_{DD}=7V and V_{th}=2.7V the noise margins are:

$$NM_H = V_{OH} - V_{IH} \qquad NM_L = V_{IL} - V_{OL}$$

$$NM_H = 7 - 3.827 = 3.173V \qquad NM_L = 3.085 - 0 = 3.085V$$

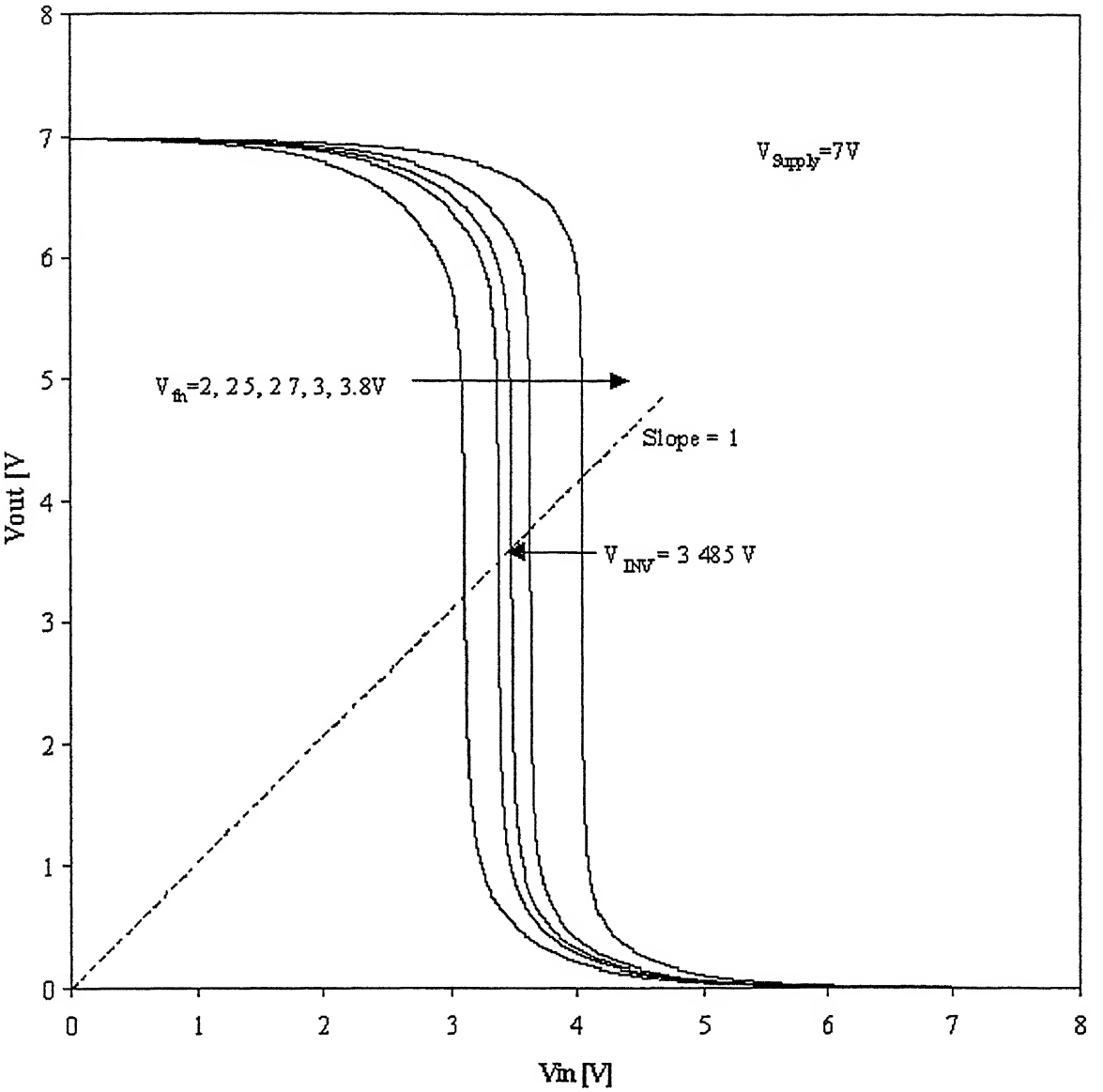

Fig 3 1 3 Inverter transfer characteristics with a 7V supply Also shown are the simulated transfer characteristics as a function of the threshold voltage of the n-channel transistor.

For the transient analysis an inverter chain as shown below is used

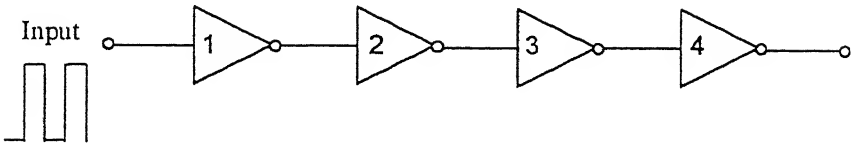

Fig 3 1 4 Series of Inverters

The inverter chain is required not only to measure the delays for abrupt input transition but also for more realistic gradually varying input transitions. In figure 3 1 3 a series of inverter is shown and a step input is applied at the input of the first inverter

The simulation result for the Inverter no 1 is

$t_{0PHL} = 123ns$ $t_{0PLH} = 188ns$

where t_{0PHL} is the high to low and t_{0PLH} is the low to high delay for abrupt input

For the inverter no 3 the input transitions is

$t_{ir} = 450ns$ $t_{if} = 295ns$

where t_{ir} is the rise time and t_{if} is the fall time of the input

The measured delays are

$t_{PHL} = 290ns$ $t_{PLH} = 277ns$

where t_{PHL} is high to low and t_{PLH} is low to high delay for the input with rise and fall time given above

The simulation result for the inverter no 3 is shown in figure 3.1.4.

Now a very simple model of a gate that describes the dependence of delay upon the input rise and fall time is given by the expression [8].

$$t_{PHL} = \sqrt{(t_{0PHL})^2 + \left(\frac{t_{ir}}{2}\right)^2} \quad \text{..... (3 1)}$$

$$t_{PLH} = \sqrt{(t_{0PLH})^2 + \left(\frac{t_{if}}{2}\right)^2} \quad \text{..... (3.2)}$$

$$t_{PHL} = \sqrt{(123)^2 + \left(\frac{450}{2}\right)^2} \qquad t_{PLH} = \sqrt{(188)^2 + \left(\frac{295}{2}\right)^2}$$

$$t_{PHL} = 256.5\text{ns} \qquad t_{PLH} = 239\text{ns}$$

The SPICE results and the calculated results are approximately equal.

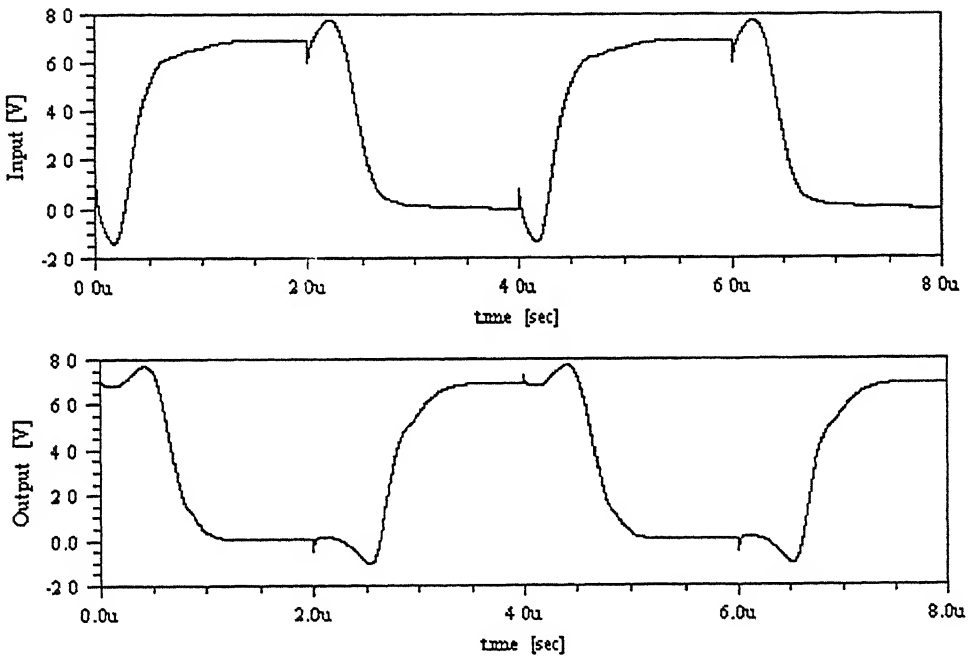

Fig 3.1.4 transient characteristics of inverter

A very simple model of delay that describes its dependency upon the load capacitance, pull up (down) current is given by the expression

$$t_{PHL}(t_{PLH}) = \frac{C_{Total}\,\frac{V_{DD}}{2}}{I_{DN}(I_{DP})} \qquad \text{.....(3.3)}$$

Where I_{DN} is the pull down and I_{DP} is the pull up current. C_{Total} is the total capacitance at the output node, which is the sum of load capacitance and the capacitance of the inverter.

in **Appendix B**. I_{DN} and I_{DP} are measured using separate n-channel TFT and p-channel TFT. The conditions for measuring the currents are: For a-Si TFT, the gate and drain was at 7V keeping source at ground and For pentacene p-channel TFT, the gate and drain was at 0V with source at 7V.

The calculated delays are

$$t_{PLH} = \frac{0.64\times10^{-15}\times3.5}{1.5\times10^{-8}} = 150\text{ns} \qquad t_{PHL} = \frac{0.64\times10^{-15}\times3.5}{2.25\times10^{-8}} = 99.5\text{ns}$$

These calculated values of delays are approximately equal to the measured values of the delays. The error is because the charging and discharging currents are assumed to be constant and maximum.

As mentioned earlier that the delay of gate is a function of the load capacitance. A very simple model of delay can also be expressed as

$$t_{PLH} \text{ or } t_{PHL} = a + b \times C_L \qquad \text{.....(3.4)}$$

Where a = Intrinsic rise (fall),

b = rise (fall) resistance, and

C_L = load capacitance.

a = t_{PHL} or t_{PLH} for C_L=0 and

b = slope of the line plotted between delay and C_L.

To estimate these parameters, it is needed to measure the delays for different capacitive load and plot the delays vs. capacitance. The delays for the inverter, for different capacitive loads are measured and given in the following table.

Delays with capacitive load:

Switching characteristics					
Symbol	Parameter	**Nom. V_{DD}=5V, T_A=25 °C**			
		C_L=0.1fF	C_L=0.2fF	C_L=0.4fF	C_L=0.6fF
t_{PHL}	Propagation delay	187.5	222	257	283
t_{PLH}	A to Output (ns)	204	244	281	311
t_{or}	Output transition	161	219	280	335
t_{of}	time	150	194	237	273
t_{ir}	Input transition	467	489	497	468
t_{if}	time	340	311	299	290

A plot of delay Vs capacitive load was plotted and the measured values are:

Intrinsic rise = 170.5ns rise resistance = 358MΩ

Intrinsic fall = 157ns fall resistance = 321.5MΩ

3.2 NAND Gate:

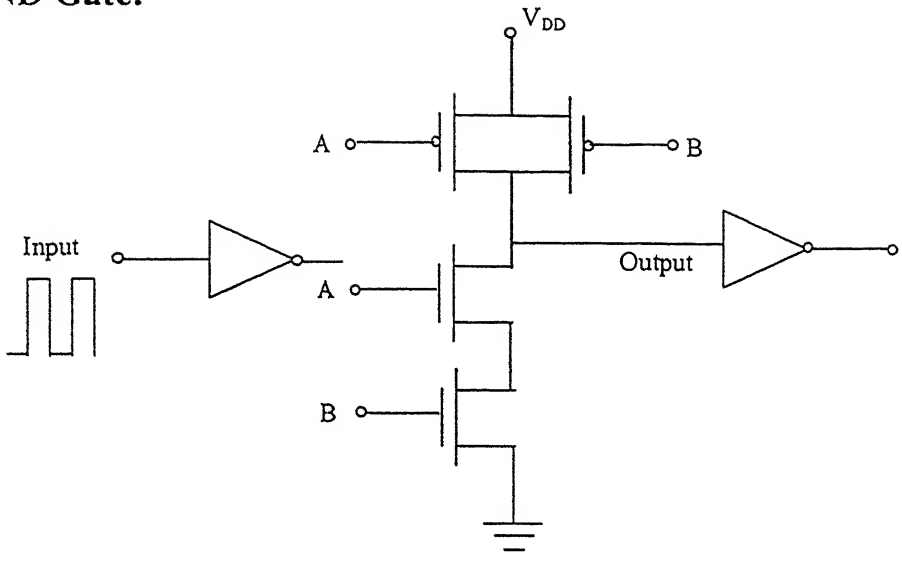

Fig 3.2.1 NAND gate circuit

The NAND gate circuit is shown in the above figure 3.1.1. Two p-channel TFTs are connected in parallel and two n-channel TFTs are in series. The channel dimensions of the a-Si n-channel TFTs are W=2μm, L=1μm and of the Pentacene p-channel TFTs are W=1μm, L=1μm. Because of two n-channel TFTs are connected in series, the effective resistance will be double hence the delay will be double. To reduce this resistance the channel width has to be made double. That's why the channel width of the n-channel TFTs is doubled.

For the measurement of the delay an inverter is connected at the input as a driver and an inverter is connected at the output as a load.

There are three conditions for applying input. Generally the condition when both input are varying is not used. The other two input conditions are explained as

1. When input A=7V and B is changing from 0V to 7V.

The delays measured for the input with zero rise and fall time is

t_{PHL} = 228ns t_{PLH} = 500ns

Here in this case for the p-channel TFT, transistor A is off and transistor B is going to be OFF, so the net pull up current flowing through these transistor will be decreasing. But in the case of n-channel TFT transistor A is ON and B is going to be ON, hence the pull down current will be increasing. This is the reason why t_{PLH} is greater than t_{PHL}.

Now the driver inverter is connected at input B. The transition of the input at node B (Output of the driving inverter) (fig 3.3.2):

$t_{ir} = 624ns$ $t_{if} = 298ns$

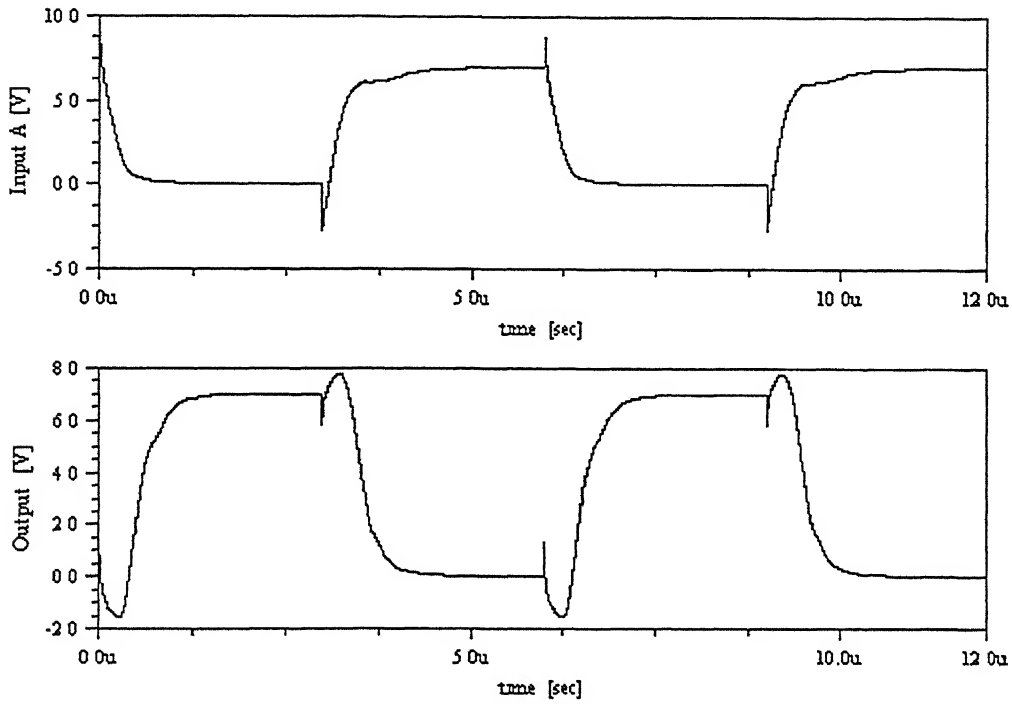

Fig 3.2.2 switching characteristics of NAND gate

The delays with output rise and fall times are

$t_{PHL} = 422ns$ $t_{of} = 462ns$

$t_{PLH} = 593ns$ $t_{or} = 766ns$

For the case of abrupt input the t_{PLH} is approximately double of t_{PHL}. But here due to the input rise and fall times the t_{PLH} is not much greater than t_{PHL}.

With the equation **3.1** and **3.2** the calculated delays are

$$t_{PHL} = [(228)^2 + (624/2)^2]^{1/2} = 386ns$$

$$t_{PLH} = [(500)^2 + (298/2)^2]^{1/2} = 521ns$$

These calculated values are approximately equal to the measured values of the delays. The calculation of the capacitance at the output node is a complex job in this case hence it is difficult to calculate the delays with the load capacitance model, given in equation 3.3.

2. When input B=7V and A is changing from 0V to 7V.

The delay with zero rise and fall time of the input

$t_{PHL} = 197ns$ $t_{PLH} = 280ns$

Now the driver inverter is connected at input A. The transition of the input at node A (the output of the driving inverter):

$t_{ir} = 787ns$ $t_{if} = 346ns$

The delays with output rise and fall times are

$t_{PHL} = 325ns$ $t_{of} = 448ns$

$t_{PLH} = 378ns$ $t_{or} = 494ns$

And with the equation **3.1** and **3.2** the calculated values of the delays are

$$t_{PHL} = [(197)^2 + (787/2)^2]^{1/2} = 440ns$$

$$t_{PLH} = [(280)^2 + (346/2)^2]^{1/2} = 329ns$$

These calculated values are also approximately equal to the measured values of the delays. The error coming in the case of t_{PHL} is due to the error in the rise time. The simulator gives some distortion for the rising edge of the input.

It can be seen that the delays for input A is less than the delay for input B as it is also in the case of CMOS NAND gate. As it is explained that the delay of any gate depends upon the output capacitance. The total capacitance for the input A is the load capacitance only but for the input B the total capacitance will be the sum of load

capacitance and the capacitance at the node between two n-channel TFT. Thus the capacitance for the input B is greater than the capacitance for the input A. hence the delay for input A is less than the delay for input B.

Delays with capacitive load:

(i) Propagation delay (input A to Output)

C_L (fF)	t_{PHL}(ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	226	250	302	202	702	393
0.2	256	280	345	260	715	363
0.3	288	325	382	320	750	351
0.4	316	363	414	373	761	343

(ii) Propagation delay (input B to Output)

C_L (fF)	t_{PHL}(ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	337	295	514	452	708	310
0.2	370	322	550	522	702	306
0.3	394	360	585	585	697	306
0.4	414	388	604	655	672	304

The input rise and fall time for different capacitive load is different because the load capacitance also affects the delay of driving inverter.

A plot of delay Vs capacitive load was plotted and the measured values are:

For input A:

Intrinsic rise = 267ns rise resistance = 373MΩ

Intrinsic fall = 196ns fall resistance = 302MΩ

For input B:

Intrinsic rise = 487ns rise resistance = 305MΩ

Intrinsic fall = 315ns fall resistance = 255MΩ

3.3 NOR Gate:

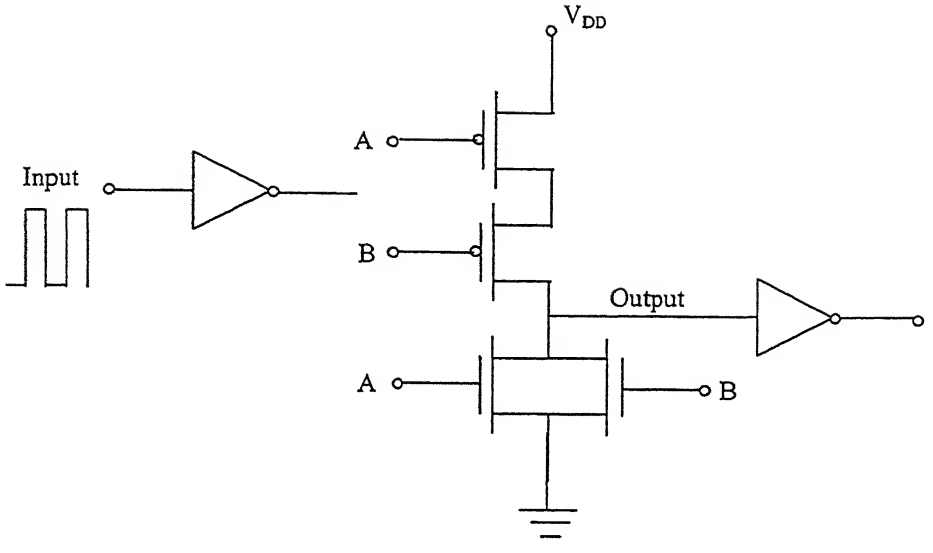

Fig 3.3.1 NOR gate circuit

The above fig 3.3.1 is NOR gate circuit. The channel dimensions of the a-Si n-channel TFTs are W=1μm, L=1μm and of the Pentacene p-channel TFTs W=2μm, L=1μm. Because the two p-channel TFT are connected in series the resistance will be double hence the delay will be doubled. To decrease the delay the channel width of the p-channel TFT has chosen double.

For measuring the delay one inverter is connected at the input as a driver and one inverter is connected at the output as a load.

Here also there are three conditions for giving input but the condition when both inputs are varying is generally not used. The other two conditions for applying input are:

1. When input A=0V and B is changing from 0V to 7V.

   For the input with zero rise and fall time the delays are

$$t_{PHL} = 149ns \qquad t_{PLH} = 248ns$$

Here p-channel TFT for input A will be ON as input A is at ground and p-channel TFT for input B will be going to be OFF as B is changing from 0V to 7V. So the net current flowing through p-channel TFT will be decreasing. But for n-channel TFT the net current

greater than t_{PHL}

Now the driver inverter is connected at node B. the input transitions at the node B (output of the driving inverter) is [Fig 3 3 2 (a)]

t_{ir} = 495ns t_{if} = 230ns

The delays with the output rise and fall times are

t_{PHL} = 361ns t_{of} = 380ns

t_{PLH} = 303ns t_{or} = 602ns

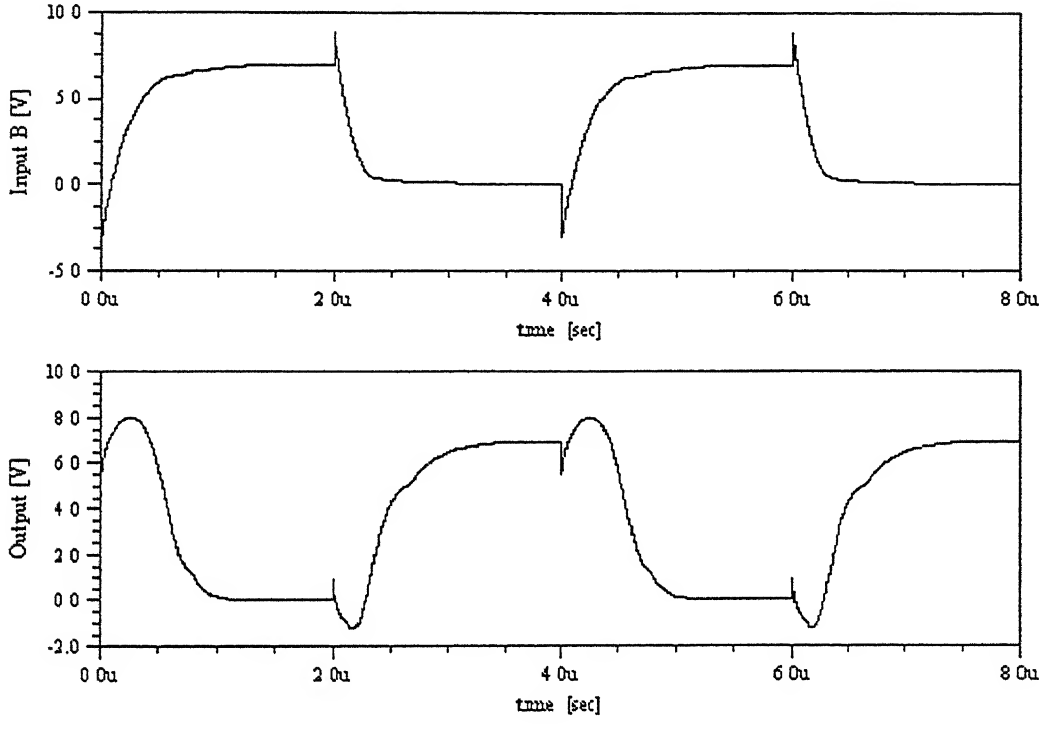

Fig 3.3 2 Switching characteristics of NOR gate

Again the calculation of delays with the equation **3.1** and **3.2** are

$$t_{PHL} = [(149)^2 + (495/2)^2]^{1/2} = 289ns$$

$$t_{PLH} = [(248)^2 + (230/2)^2]^{1/2} = 273ns$$

The measured values and the calculated values of the delays are approximately equal

2. When input B=0V and A is changing from 0V to 7V.

For zero rise and fall time of the input the delays are

$t_{PHL} = 223ns$ $t_{PLH} = 260ns$

Now the driver inverter is connected at A. The input transitions at the node A are

$t_{ir} = 422ns$ $t_{if} = 268ns$

The delays are

$t_{PHL} = 416ns$ $t_{of} = 460ns$

$t_{PLH} = 337ns$ $t_{or} = 596ns$

And the calculation of delays with the equation **3.1** and **3.2** are

$$t_{PHL} = [(223)^2 + (422/2)^2]^{1/2} = 307ns$$

$$t_{PLH} = [(260)^2 + (268/2)^2]^{1/2} = 292.5ns$$

The calculated values and the measured values are approximately equal.

The delay for input A is greater than the delay for input B, as it is also in the case of CMOS NOR gates.

Delays with capacitive load:

(i) Propagation delay (input A to Output)

C_L (fF)	t_{PHL}(ns)	t_{of}(ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	339	275	260	280	467	290
0.2	365	313	296	335	447	278
0.3	383	350	333	396	432	271
0.4	404	390	364	457	422	269

(ii) Propagation delay (input B to Output)

C_L (fF)	t_{PHL}(ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	266	193	228	282	584	242
0.2	298	226	264	340	588	233
0.3	328	263	300	404	591	226
0.4	353	300	334	465	544	220

A plot of delay Vs capacitive load was plotted and the measured values are:

For input A:

Intrinsic rise = 226ns rise resistance = 349MΩ

Intrinsic fall = 319ns fall resistance = 213MΩ

For input B:

Intrinsic rise = 193ns rise resistance = 354MΩ

Intrinsic fall = 238.5ns fall resistance = 291MΩ

3.4 AND Gate:

The circuit for AND gate, similar to the circuit of NAND gate, is shown in figure3.4.1. One inverter is connected at the output of the nand gate for loading. The a-Si n-channel TFT's channel dimensions are W=2μm, L=1μm. and the channel dimensions of pentacene p-channel TFTs are W=1μm, L=1μm. For measuring the delay one inverter is connected at the input as a driver and an inverter is connected as a load. The inverter channel dimensions are *W*=1μm and *L*=1μm for a-Si TFT and *W*=1μm and *L*=1μm for pentacene TFT.

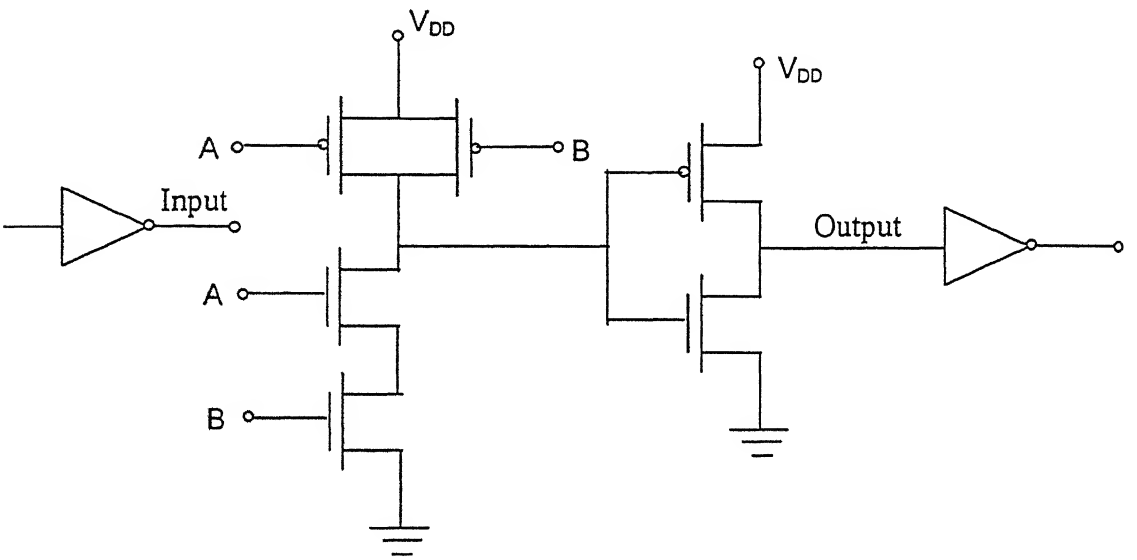

Fig 3.4.1 AND gate

The two conditions for giving input are:

1. When input A=7V and B is changing from 0V to 7V.

For abrupt rise and fall of the input the delays are

t_{PHL} = 837ns t_{PLH} = 519ns

Now the driving inverter is connected at B and the input transitions at node B are

t_{ir} = 631ns t_{if} = 300ns

The delays with output rise and fall times are

$t_{PHL} = 940ns$ $t_{of} = 409ns$

$t_{PLH} = 744ns$ $t_{or} = 501ns$

2. When input B=7V and A is changing from 0V to 7V.

For abrupt rise and fall of the input the delays are

$t_{PHL} = 582ns$ $t_{PLH} = 510ns$

The input transitions at node A are (driving inverter is connected at A)

$t_{ir} = 780ns$ $t_{if} = 347ns$

The delays with output rise and fall times are

$t_{PHL} = 695ns$ $t_{of} = 365ns$

$t_{PLH} = 648ns$ $t_{or} = 512ns$

3.5 OR Gate:

One inverter is connected at the output of the NOR gate. The circuit of an OR gate is shown in fig 3.5.1. The a-Si n-channel TFT's channel dimensions are W=1μm, L=1μm. and the channel dimensions of p-channel pentacene TFTs are W=2μm, L=1μm. These channel dimensions are chosen to make the delays nearly equal. To drive the gate an inverter is connected at the input. And the simulation results have been taken for the load of an inverter.

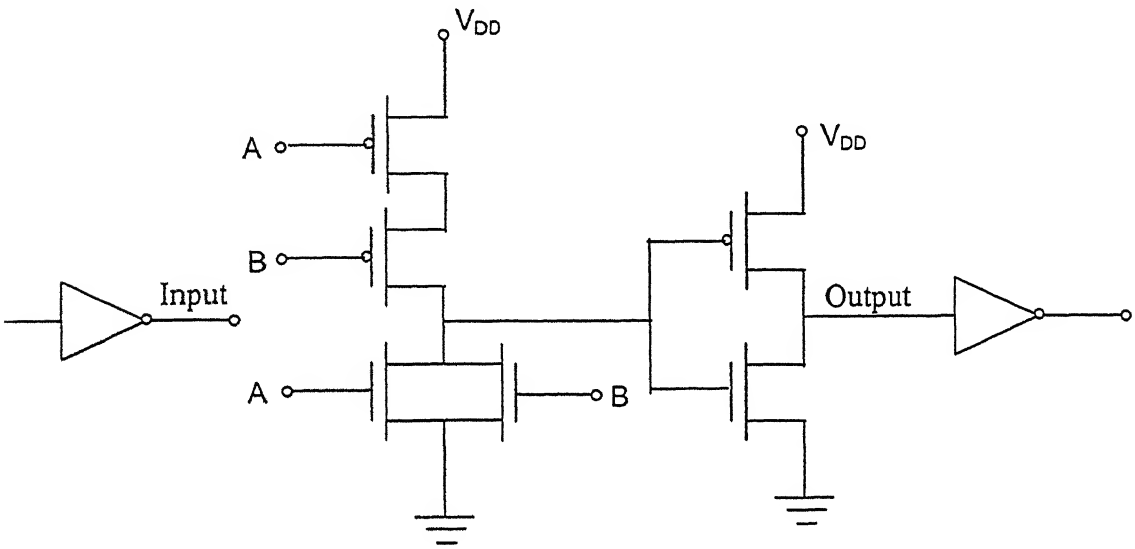

Fig 3.5.1 OR gate circuit

Here also there will be two conditions for applying input

1. When input A=0V and B is changing from 0V to 7V.

For abrupt rise and fall of the input the delays are

$t_{PHL} = 585ns$ $t_{PLH} = 433ns$

The input transitions are

$t_{ir} = 478ns$ $t_{if} = 227ns$

The delays with output rise and fall times are

$t_{PHI} = 649ns$ $t_{of} = 395ns$

$t_{PLH} = 653ns$ $t_{or} = 476ns$

2. When input B=0V and A is changing from 0V to 7V.

For abrupt rise and fall of the input the delays are

$t_{PHL} = 602ns$ $t_{PLH} = 510ns$

The input transitions are

$t_{ir} = 418ns$ $t_{if} = 274ns$

The delays with output rise and fall times are

$t_{PHL} = 680ns$ $t_{of} = 395ns$

$t_{PLH} = 717ns$ $t_{or} = 482ns$

Similar to the above designs of the logical circuits AOI, D-FF, XOR have designed and their delays are measured for capacitive load.

3.6 AND-OR-INVERT:

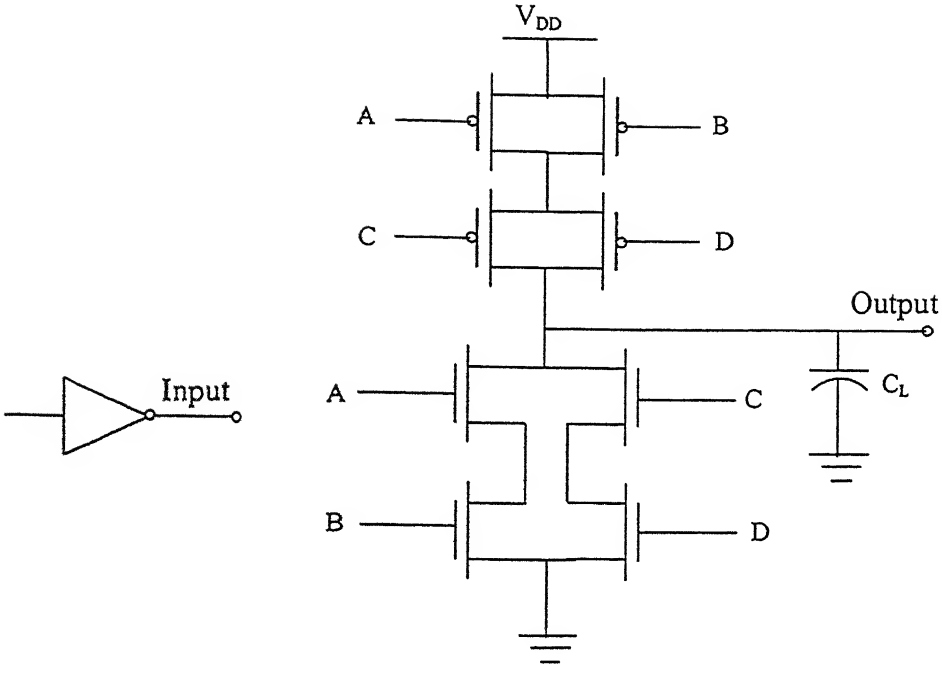

Fig 3.6 AOI

The above circuit is an AND-OR-INVERT circuit. The channel dimension of the P-channel pentacene TFTs are W=4μm, L=1μm. and for the n-channel a-Si TFTs W=2μm, L=1μm. Capacitive load C_L is connected at the output. For measuring the delay one inverter is connected at the input as a driver.

There are many conditions for applying input. Some conditions are explained as

Delays with capacitive load:

(i) Propagation delay (input A to Output with B=C=7V, D=0V)

C_L (fF)	t_{PHL}(ns)	t_{of}(ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	619	937	432	440	703	505
0.2	645	970	446	464	694	497
0.3	658	999	466	500	680	500
0.4	676	995	481	525	683	490

(ii) **Propagation delay (input B to Output with A=C=7V, D=0V)**

C_L (fF)	t_{PHL} (ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	695	853	530	570	850	473
0.2	719	888	544	607	848	474
0.3	745	931	562	639	846	478
0.4	750	941	574	663	849	475

(iii) **Propagation delay (input C to Output with A=D=7V, B=0V)**

C_L (fF)	t_{PHL} (ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	443	746	390	445	843	414
0.2	472	786	410	473	846	412
0.3	485	764	429	505	855	407
0.4	523	819	447	539	818	409

(iv) **Propagation delay (input D to Output with A=C=7V, B=0V)**

C_L (fF)	t_{PHL} (ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (ns)	t_{if} (ns)
0.1	527	720	487	588	917	389
0.2	552	729	502	624	914	389
0.3	584	743	519	649	902	387
0.4	601	777	537	680	890	388

A plot of delay Vs capacitive load was plotted and the measured values are:

For input A:

Intrinsic rise = 414.5ns rise resistance = 167MΩ

Intrinsic fall = 603.5ns fall resistance = 184MΩ

For input B:

Intrinsic rise = 515ns rise resistance = 150MΩ

Intrinsic fall = 679.5ns fall resistance = 191MΩ

For input C:

Intrinsic rise = 371.5ns rise resistance = 190MΩ

Intrinsic fall = 417.5ns fall resistance = 253MΩ

For input D:

Intrinsic rise = 469.5ns rise resistance = 167MΩ

Intrinsic fall = 502.5ns fall resistance = 254MΩ

3.7 EX-OR:

The circuit of AOI can also be used as an EX-OR circuit by connecting the invert of A and B to C and D respectively.

(i) Propagation delay (input A to Output with B=7V)

C_L (fF)	t_{PHI} (ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (µs)	t_{if} (ns)
0.1	491	750	290	372	1.32	7.59
0.2	517	792	313	403	1.35	763
0.3	544	824	335	431	1.33	766
0.4	573	871	358	457	1.34	766

(ii) Propagation delay (input B to Output with A=7V)

C_L (fF)	t_{PHL} (ns)	t_{of} (ns)	t_{PLH} (ns)	t_{or} (ns)	t_{ir} (µs)	t_{if} (ns)
0.1	650	670	455	480	1.36	673
0.2	668	705	472	512	1.36	661
0.3	690	736	492	538	1.34	662
0.4	707	777	507	571	1.34	654

The measured parameters for input A:

Intrinsic rise = 267.5ns rise resistance = 226MΩ

Intrinsic fall = 463ns fall resistance = 273MΩ

For input B:

Intrinsic rise = 437.5ns rise resistance = 176MΩ

Intrinsic fall = 630.5ns fall resistance = 193MΩ

3.8 D-Latch:

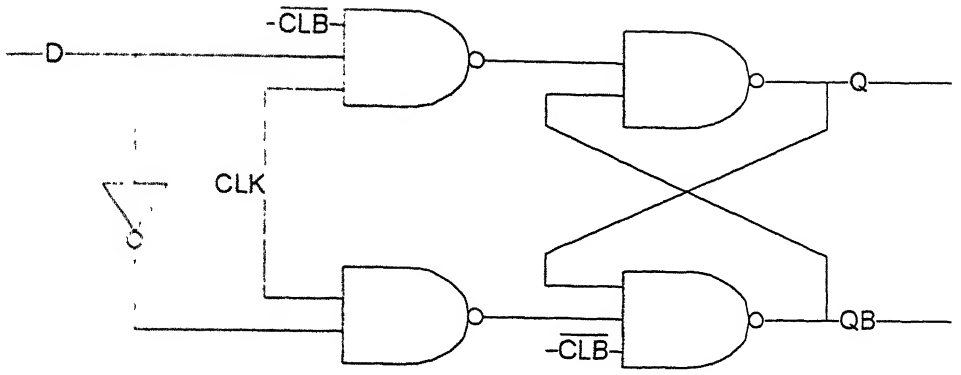

Fig 3 8.1 D-Latch

The circuit contains two 3-input NAND gates and two 2-input NAND gates and an inverter The channel dimensions for 3-input nand gate Pentacene p-channel TFT is W/L=1μm/1μm and a-Si n-channel TFT is W/L=3μm/1μm. For 2-input nand gate the a-Si n-channel TFT dimension is W/L=2μm/1μm and pentacene p-channel TFT is W/L=1μm/1μm. At the output Q and QB capacitive loads are connected and delay are measured. CLB is the clear input and CLK is clock input. A low level at the clear input make the output Q at low level and QB at high level regardless of the levels of the other inputs. When clear is inactive (high) and the clock is high, data at the D input are transferred to the output

(i) Propagation delay (CLK to Q)

C_L (fF)	t_{PHL}(μs)	t_{of}(ns)	t_{PLH} (μs)	t_{or} (μs)
0 1	1.711	753	1.089	0.945
0.2	1 786	794	1.132	1.003
0 3	1.859	848	1 166	1 041
0.4	1.907	876	1.207	1.120

(ii) **Propagation delay (CLK to QB)**

C_L (fF)	t_{PHL} (µs)	t_{of} (ns)	t_{PLH} (µs)	t_{or} (ns)
0.1	1.852	828	0.960	823
0.2	1.924	880	0.989	875
0.3	1.995	916	1.031	931
0.4	2.067	962	1.064	983

(iii) **Propagation delay (CLB to Q and QB)**

C_L (fF)	CLB to Q		CLB to QB	
	t_{PHL} (µs)	t_{of} (ns)	t_{PLH}(µs)	t_{or} (ns)
0.1	1.758	665	859	1.86
0.2	1.819	705	890	1.928
0.3	1.889	745	919	1.976
0.4	1.952	792	947	2.03

The measured parameters for CLK to Q:

Intrinsic rise = 1.0515µs rise resistance = 388MΩ

Intrinsic fall = 1.6505µs fall resistance = 661MΩ

The measured parameters for CLK to QB:

Intrinsic rise = 0.9225µs rise resistance = 354MΩ

Intrinsic fall = 1.7805µs fall resistance = 716MΩ

The measured parameters for CLB to output:

CLB to Q Intrinsic fall = 1.6915µs fall resistance = 652MΩ

CLB to QB Intrinsic rise = 0.8305µs rise resistance = 293MΩ

CHAPTER 4

Synthesis of Larger Circuits

4.1 Introduction:

Synthesis is defined as a translation from a behavioral description into a structural, similar to the compilation of programming languages such as C or Pascal into an assembly language. Each component in the structural description is in turn defined by its own behavioral description. Synthesis, sometimes called design refinement, adds an additional level of detail that provides information needed for the next level of synthesis or for manufacturing of the design.

Logic synthesis translates Boolean expressions into a netlist of components from a given library of logic gates such as NAND, NOR, EXOR, AND-OR-INVERT, and OR-AND-INVERT. This library is known as Technology Library. The target technology introduces a set of constraints imposed on the corresponding design implementation. Here technology library is made with the gate Inverter, NAND, NOR, EXOR, AND-OR-INVERT and D-Latch of thin film transistor technology using the parameters intrinsic rise (fall) and rise (fall) resistance measured in the previous chapter.

Hardware description languages are used to describe the behavior or structure of systems either on a chip level or board level. The language constructs should allow an unambiguous description for each design.

4.2 Synthesis of larger circuits:

Some logic circuits are synthesized by using two different libraries (1) TFT technology library and (2) 1.5u CMOS library. And their delays are compared in the table 4.1

4.2.1 Synthesis of 8-bit microprocessor:

The microprocessor has the following pins as shown in figure 4.2.1

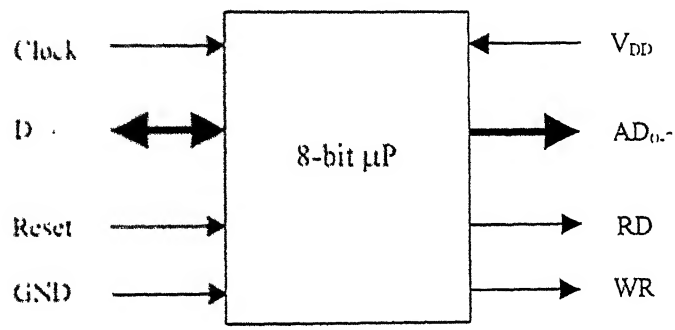

Fig 4.2.1 8-bit microprocessor

The address and data bus are of 8-bit and the microprocessor is for 8-instructions The instructions are

1. LDA address load accumulator with the contents of memory location specified by the address
2. STA address store the contents of accumulator in the memory location specified by the address.
3. MVI data load accumulator with the data specified in the next byte of instruction.
4. ADD address: add accumulator content with the contents of the specified memory location.
5. ADI address: add accumulator content with the data specified in the next byte of instruction.
6. SLA. shift left the content of the accumulator.
7. SLR. shift right the content of the accumulator.

8 JMP address jump to the address location specified and start execution from there

Architecture of the processor:

The architecture of the microprocessor is shown in the figure 4 2 2 The architecture is commonly viewed as consisting of a data path and a control unit The data path is a piece of hardware where all data manipulation takes place The sequencing of operation is done under the supervision of control unit

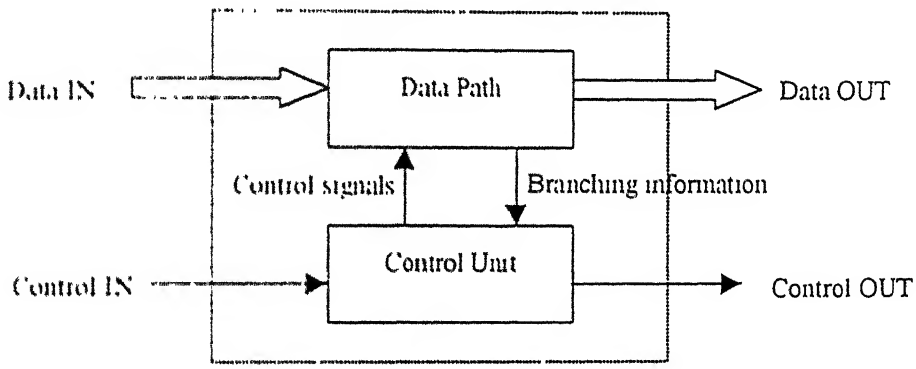

Fig 4 2 2 Architecture of microprocessor

- Accumulator: Accumulator is an 8-bit register, which stores a data as well as performs logical operations on it. After the process of the ALU data gets stored in accumulator

- Instruction Register (IR): The primary function of an instruction register is to store the instruction, data or an address

- Data Path The data path consists of storage units (or registers), functional units (like adder, multiplier etc) and interconnects unit (like multiplexers). The data path is shown in figure 4 2.3

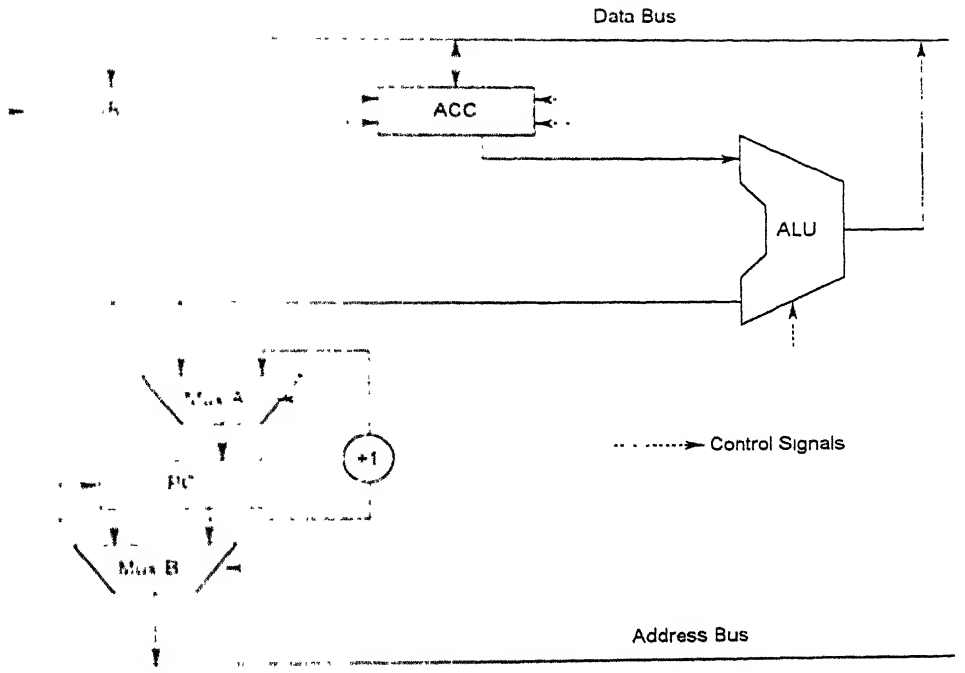

Fig 4.2 3 Data Path

- Arithmetic/ Logic Unit (ALU): It is the major functional unit of the processor It is a combinational unit used to carry out the 8-bit arithmetic/ logical operations Here the ALU is a simple 8-bit carry-look ahead adder The delay shown in the table is the worst case delay from A input to the carry out

Table 4.1 Comparison of the delays using two different libraries

Sl No	Name of the circuit	Delays measured with synthesis tool	
		TFT library (μs)	1 5μCMOS library (ns)
1	Full adder	2 609	4 41
2	8-bit multiplexer	6 516	5 55
3	8-bit multiplier (shift & Add)	81 275	105 04
4	Accumulator	3 075	3 76
5	Carry look ahead Adder (8-bit)	18 756	24 47
7	Instruction Register	3 075	3 66
8	Program Counter	4 81	4 43
9	8-bit microprocessor	40 746	48 39

- Full Adder The delay measured by the synthesis, shown in the table is the worst case delay of full adder This delay is from B input to the Carry out

- 8-bit multiplier: Shift and add logic has been used in this multiplier. Here the delay shown in the table is the worst-case delay of the multiplier from the multiplicand input to the result (output)

CHAPTER 5

CONCLUSION & FUTURE SCOPE

Conclusion:

The performance of complementary a-Si / pentacene TFT circuits has been described in detail in this work. It was shown that basic gates with good static characteristic can be obtain using this technology. The delays estimated for the gate were however large due to lower carrier mobility. For a 2-input NAND gate a delay of 500ns was estimated for a TFT gate length of 1µm. This value has to be contrasted with a delay of 0.54ns that can be obtain using 1.5µm bulk CMOS technology. For more complex circuits, a similar trend has been obtained. The results indicate that a simple 8-bit microprocessor would run only at 250kHz.

Future Scope:

The model used for pentacene TFT in the circuits is same as that for amorphous-Silicon TFT. Although this model gives a reasonable fit to the experimental characteristic, a better model specially tailored for pentacene TFT is required.

The present technology library consists of only six components Inverter, NAND, NOR, AOI, EX-OR, and D-Latch More elements need to be added to the library for the better optimization of the circuits

Appendix – A

Table A-1: Model parameters for a-Si thin film transistor

Name	Parameter	Unit	Value
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.35
EMU	Field effect mobility activation energy	eV	0.06
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states		1E23
IOL	Zero bias leakage current	A	3E-14
KASAT	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	Output conductance parameter	1/V	0
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2/Vs	0.0001
RD	Drain resistance	W	0.0
RS	Source resistance	W	0.0
SIGMA0	Minimum leakage current parameter	A	1E-14
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.7e-7
V0	Characteristic voltage for deep states	V	0.12
VAA	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero-bias threshold voltage	V	2.7

The model for Pentacene TFT was taken the same as the model for a-Si TFT by changing the parameter values, which are given in table A-2.

Table A-2: Model parameters for Pentacene thin film transistor

ALPHASAT	0.6	GMIN	1E23	TNOM	27
CGDO	0.0	IOL	3E-14	TOX	1 7e-7
CGSO	0.0	KASAT	0 006	V0	0.12
DEF0	0.6	KVT	-0.036	VAA	1.9E4
DELTA	5	LAMBDA	0	VDSL	7
EL	0.35	M	4	VFB	-3
EMU	0.06	MUBAND	0.0001	VGSL	7
EPS	2.5	RD	5E4	VMIN	0.3
EPSI	3.9	RS	5E4	VTO	-2
GAMMA	0.38	SIGMA0	1E-14		

Appendix – B

Calculation of Input Capacitance

Input capacitance of an Inverter:

The channel dimensions: (1) the channel dimension of n-channel a-Si TFTs are W= 1μm and L=1μm (2) the channel dimension of p-channel pentacene TFTs are W=33μm and L=1μm. Inverter is driven by an Inverter. The figure A-2.1 below shows the circuit for capacitance calculation

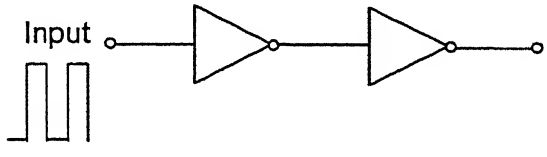

Fig. A-2.1 Circuit for Current measurement

The current at the node between inverters is plotted and the capacitance at this node will be approximately the capacitance of the inverter.

Measured Input capacitance C = area of the curve/ V

$$C = 0.64\text{fF}$$

Input capacitance calculated with oxide thickness

$$C_{in} = C_{oxP} + C_{oxN}$$

$$= \frac{\varepsilon_{ox} W_P \times L_P}{t_{oxP}} + \frac{\varepsilon_{ox} W_N \times L_N}{t_{oxN}}$$

$$= 0.59\text{fF}$$

The capacitance measured by aim-spice is approximately equal to the calculated value.

The input capacitances for other gates except inverter are calculated by calculating the oxide capacitances because in their case it is difficult to measure the capacitance with transient current plot. The calculated input capacitances are given in the following table:

Gate circuit		Input capacitance(fF)
NAND		0.973
NOR		0.791
AOI		1.58
EX-OR		2.22
D-latch	D input	1.36
	Cloak input	2.33
	Clear input	2.72

Synopsys Technology Library

```
library(tft) {
      date : "Jan 22, 2002";
      revision : 1.0;

    default_inout_pin_cap        :  1.0;
    default_inout_pin_fall_res   :  0.0;
    default_inout_pin_rise_res   :  0.0;
    default_input_pin_cap        :  1.0;
    default_intrinsic_fall       :  1.0;
    default_intrinsic_rise       :  1.0;
    default_output_pin_cap       :  0.0;
    default_output_pin_fall_res  :  0.0;
    default_output_pin_rise_res  :  0.0;
    default_slope_fall           :  0.0;
    default_slope_rise           :  0.0;
    default_fanout_load          :  1.0;

    default_wire_load_capacitance : 1.0;
    default_wire_load_resistance : 1.0;
    default_wire_load_area       : 1.0;

    k_process_drive_fall         :  1.0;
    k_process_drive_rise         :  1.0;
    k_process_intrinsic_fall     :  1.0;
    k_process_intrinsic_rise     :  1.0;
    k_process_pin_cap            :  0.0;
    k_process_slope_fall         :  1.0;
    k_process_slope_rise         :  1.0;
    k_process_wire_cap           :  0.0;
    k_process_wire_res           :  1.0;
    k_temp_drive_fall            :  0.0037;
    k_temp_drive_rise            :  0.0037;
    k_temp_intrinsic_fall        :  0.0037;
    k_temp_intrinsic_rise        :  0.0037;
    k_temp_pin_cap               :  0.0;
    k_temp_slope_fall            :  0.0;
    k_temp_slope_rise            :  0.0;
    k_temp_wire_cap              :  0.0;
    k_temp_wire_res              :  0.0;
    k_volt_drive_fall            : -0.26;
    k_volt_drive_rise            : -0.26;
    k_volt_intrinsic_fall        : -0.26;
    k_volt_intrinsic_rise        : -0.26;

    k_volt_pin_cap               :  0.0;
    k_volt_slope_fall            :  0.0;
    k_volt_slope_rise            :  0.0;
    k_volt_wire_cap              :  0.0;
    k_volt_wire_res              :  0.0;

    time_unit : "1ns";
```

```
    voltage_unit : "1V";
    current_unit : "1uA";
    pulling_resistance_unit : "1kohm";
    capacitive_load_unit (1,pf);

    nom_process                    :  1.0;
    nom_temperature                : 25.0;
    nom_voltage                    :  3.3;

     in_place_swap_mode : match_footprint;

    wire_load("05x05") {
        resistance : 0 ;
        capacitance : 0.001 ;
        area : 0 ;
        slope : 0.186 ;
        fanout_length(1,0.39) ;
    }
    wire_load("10x10") {
        resistance : 0 ;
        capacitance : 0.001 ;
        area : 0 ;
        slope : 0.311 ;
        fanout_length(1,0.53) ;
    }
    wire_load("20x20") {
        resistance : 0 ;
        capacitance : 0.001 ;
        area : 0 ;
        slope : 0.547 ;
        fanout_length(1,0.86) ;
    }

    wire_load_selection() {
      wire_load_from_area(0,1000,05x05);
      wire_load_from_area(1001,2000,10x10);
      wire_load_from_area(2001,3000,20x20);
    }

cell(inv) {
  area : 1;
  cell_footprint : "inv";
  pin(A) {
    direction : input;
    capacitance : 0.00064;
  }
  pin(OUT) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 170;
      intrinsic_fall : 154;
      rise_resistance : 360000;
      fall_resistance : 330000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
```

```
    }
  }
}


cell(nand2) {
  area : 1;
  cell_footprint : "nand2";
  pin(A) {
    direction : input;
    capacitance : 0.000973;
  }
  pin(B) {
    direction : input;
    capacitance : 0.000973;
  }
  pin(OUT) {
    direction : output;
    function : "(A B)'";
    timing() {
      intrinsic_rise : 267;
      intrinsic_fall : 196;
      rise_resistance : 373000;
      fall_resistance : 302000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 487;
      intrinsic_fall : 315;
      rise_resistance : 305000;
      fall_resistance : 255000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "B";
    }
  }
}

cell(nor2) {
  area : 1;
  cell_footprint : "nor2";
  pin(A) {
    direction : input;
    capacitance : 0.000791;
  }
  pin(B) {
    direction : input;
    capacitance : 0.000791;
  }
  pin(OUT) {
    direction : output;
    function : "(A+B)'";
    timing() {
      intrinsic_rise : 226;
      intrinsic_fall : 319;
```

```
      rise_resistance : 349000;
      fall_resistance : 213000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 193;
      intrinsic_fall : 238.5;
      rise_resistance : 354000;
      fall_resistance : 291000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "B";
    }
  }
}


cell(AOI) {
  area : 1;
  cell_footprint : "AOI";
  pin(A) {
    direction : input;
    capacitance : 0.00158;
  }
  pin(B) {
    direction : input;
    capacitance : 0.00158;
  }
  pin(C) {
    direction : input;
    capacitance : 0.00158;
  }
  pin(D) {
    direction : input;
    capacitance : 0.00158;
  }
  pin(OUT) {
    direction : output;
    function : "(A B+C D)'";
    timing() {
      intrinsic_rise : 414.5;
      intrinsic_fall : 603.5;
      rise_resistance : 167000;
      fall_resistance : 184000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 515;
      intrinsic_fall : 679.5;
      rise_resistance : 150000;
      fall_resistance : 191000;
      slope_rise : 0.0;
      slope_fall : 0.0;
```

```
      related_pin : "B";
    }
    timing() {
      intrinsic_rise : 371.5;
      intrinsic_fall : 417.5;
      rise_resistance : 190000;
      fall_resistance : 253000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "C";
    }
    timing() {
      intrinsic_rise : 469.5;
      intrinsic_fall : 502.5;
      rise_resistance : 167000;
      fall_resistance : 254000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "D";
    }
  }
}

cell(EX-OR) {
  area : 1;
  cell_footprint : "xor";
  pin(A) {
    direction : input;
    capacitance : 0.00222;
  }
  pin(B) {
    direction : input;
    capacitance : 0.00222;
  }
  pin(OUT) {
    direction : output;
    function : "(A B' + A' B)";
    timing() {
      intrinsic_rise : 267.5;
      intrinsic_fall : 463;
      rise_resistance : 226000;
      fall_resistance : 273000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 437.5;
      intrinsic_fall : 630.5;
      rise_resistance : 176000;
      fall_resistance : 193000;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "B";
    }
  }
}
```

```
cell(dffc_s) {
  area : 9;
  cell_footprint : "dffc_s";
  pin(DATA) {
    direction : input;
    capacitance : 0.001359;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.85;
      intrinsic_fall : 0.85;
      related_pin : "CLK";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CLK";
    }
  }
  pin(CLK) {
    direction : input;
    capacitance : 0.00233;
  }
  pin(CLB) {
    direction : input;
    capacitance : 0.00272;
  }

  ff("IQ","IQB") {
    next_state : "DATA";
    clocked_on : "CLK";
    clear   : "CLB'";
  }
  statetable ( "  DATA   CLK  CLB  ", " Q  QB") {
      table :"  -    -    L   : - - :  L   H, \
                  -   ~R   H   : - - :  N   N, \
                H/L   R   H   : - - : H/L L/H";
    }

  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1051.5;
      intrinsic_fall : 1650.5;
      rise_resistance : 388000;
      fall_resistance : 661000;
      related_pin : "CLK";
    }
    timing() {
      timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1691.5;
      fall_resistance : 652000;
      related_pin : "CLB";
```

```
    }
  }
  pin(QB) {
    direction : output;
    function : "IQB";
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 922.5;
      intrinsic_fall : 1780.5;
      rise_resistance : 354000;
      fall_resistance : 716000;
      related_pin : "CLK";
    }
    timing() {
      timing_type : preset;
      timing_sense : negative_unate;
      intrinsic_rise : 830.5;
      rise_resistance : 293000;
      related_pin : "CLB";
    }
  }
}
}
```

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